A Low Noise Alternative to a 3-state Phase Detector

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***Abstract*—To facilitate an application of an analog phase detector (PD) in the phase locked loop (PLL) a circuit has been designed. The pull-in range is achieved by means of the very component that constitutes the PD. Therefore, the circuit resembles a 3-state PD, which uses the same elements when locked and out of lock. Besides being simple, the proposed circuit provides PLL with low noise performance typical for an analog PD.**

***Index Terms*—PLL, frequency synthesis, low noise oscillations**

I. Introduction

There are a few techniques that utilize some auxiliary circuit (AUX) to acquire the necessary phase locked loop (PLL) pull-in range. In some designs the AUX detects the difference between the reference frequency and the voltage controlled oscillator (VCO) frequency $\Delta f = f_{VCO} - f_{ref}$ [1] (Fig. 1). Then the phase detector (PD) and AUX outputs are multiplexed by a multiplexer (MUX) to form the VCO tuning voltage V_{tune}.

All but one of such techniques presuppose an AUX *external to the PD*, with the exception being a 3-state PD (3PD) [2]. The latter performs both functions with the *same* components. This property of the 3PD provides considerable simplification of the PLL circuitry. Consequently, it gained popularity in the majority of designs.

However, when the low noise synthesis is of concern the 3PD is far *less attractive* due to the large level of its residual phase noise. In order to avoid this problem several approaches have been proposed (discussed at length in Section IV). Yet none of them is an exception from the general rule: whenever the low noise performance is achieved there is a drastic increase in complexity, and vice versa.

Therefore, for low noise applications it is preferable to develop a PLL design that, while utilizing an analog PD, requires less spare components and does not compromise other performance, such as the pull-in range and the pull-in time. The outlines of such design are given in Section II. The particular prototype is described in Section III. The distinguishing features and possible impact are analyzed in Section IV.

II. Principles of realization

For PLL to be low noise means to use a passive analog PD; to be simple and to have extended pull-in range means to make the PD a part of the AUX circuitry. As to the latter

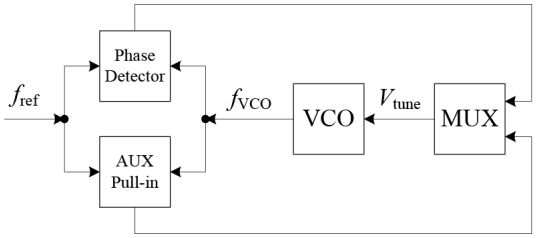

Fig. 1. The basic approach to achieve the PLL pull-in range.

it is better it be not active while Δf is comparable to the PLL bandwidth BW (*the "0" state*). While the PLL is out of lock, the AUX must reduce $|\Delta f|$ to the value comparable with BW. Evidently, for this purpose, it is sufficient to know *only* the *sign* of Δf. Each sign corresponds to one of *two other states*, namely, the pull-up and pull-down states. The proposed AUX is called here a *frequency comparator* (FC) since it functions in a way similar to a voltage comparator with one reservation mentioned later (See II C).

A. Sign of frequency difference detection

The sub-task of the Δf *sign extraction* is easily achieved by using two double balanced mixers (DBM) (Fig. 2). One pair of their corresponding inputs are fed with in-phase oscillations, another pair with oscillations in quadrature. The latter condition is not strict, allowing for some deviation from 90 degrees $\Delta\varphi_{ref}$. Whenever $|\Delta\varphi_{ref}| < \frac{\pi}{2}$, the sign of phase difference between the intermediate frequency (IF) outputs $\Delta\varphi_{IF} = \varphi_{IF_2} - \varphi_{IF_1}$ contains all information necessary to determine $sgn\,(\Delta f)$. For if $f_{VCO} > f_{ref}$ then $\Delta\varphi_{IF} = \frac{\pi}{2} + \Delta\varphi_{ref}$, if $f_{VCO} < f_{ref}$ then $\Delta\varphi_{IF} = -\frac{\pi}{2} - \Delta\varphi_{ref}$. Therefore, $sgn\,(\Delta f) = sgn\,(\Delta\varphi_{IF})$.

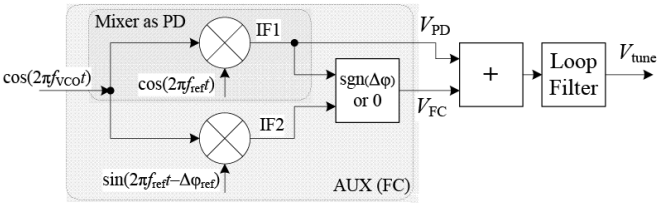

Fig. 2. The analog alternative to the 3PD.

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B. Pulling up and down

Knowing only $sgn\,(\Delta f)$ it is a reasonable strategy to change V_{tune} at the constant rate so as to reduce $|\Delta f|$. It can be realized by applying current sources to the PLL filter's capacitor. This and subsequent entries in this section presuppose the PLL with an *integrator* in the loop.

C. Switching between states

When $|\Delta f|$ is close to BW, frequency pulling need be stopped at the threshold level Δf_{thr}, and control over the tuning voltage be given to the PD. This and above-mentioned properties of the AUX are summarized in a graph in Fig. 3. It shows that, unlike a voltage comparator, the FC does not exhibit sharp transition between two extreme output levels.

There is at least one obvious way to indicate arriving at Δf_{thr}, that is, to introduce high pass filters in the IF1 and IF2 paths. To prevent FC operation below the desired Δf_{thr} cut-off frequency should be adjusted.

D. Phase and lock detection

The sub-task of *phase detection* is readily accomplished by utilizing one of the IF outputs from DC to the PLL bandwidth. Moreover, when the PLL is locked, DC voltage at the other IF output will take its most positive or negative value. This feature immediately provides the circuit with a *lock detection* signal. Therefore, *both* DBMs in the circuit are *active* while the PLL is locked and out of lock.

III. Description of the Prototype

A. PLL prototype

The proposed FC circuit was implemented in the PLL with a VCO tunable in slightly over 1 GHz range (HMC431 [3]) (Fig. 4). In subsequent experiments f_{ref} took values between 5900 MHz and 6900 MHz. The tunable oscillation is synthesized directly using a mixer and frequency divider. The high pass filter rejects the lower sideband oscillation occurring as a by-product of the direct synthesis. The PLL bandwidth BW is about 10 MHz. There is no fixed value of BW since VCO tuning slope changes fourfold in the VCO tuning range.

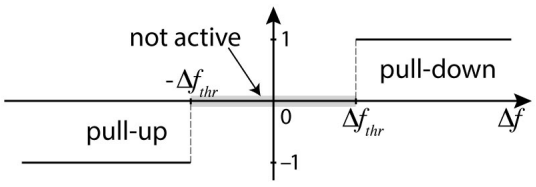

Fig. 3. The FC characteristic.

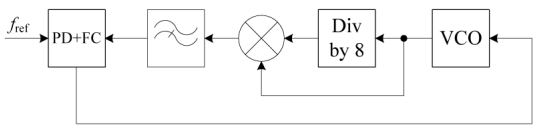

Fig. 4. The block diagram of the PLL prototype (simplified).

B. Frequency comparator

An FC was built using in-phase quadrature mixer HMC520A [4] (Fig. 5). It is accompanied by the 'sgn or 0' circuit, and the interface to the loop filter (not shown, being at the other side of the PCB). Reference oscillation is fed into the LO port of HMC520A.

To provide the correct operation of the FC it is necessary to obtain $sgn\,(\Delta\varphi_{IF})$ in the range of about two decades, i.e. 10 MHz (roughly the value of BW) to 1 GHz (roughly the range of the possible frequency tuning). This requires corresponding broadband performance of the detection circuitry. But most of broadband PDs do *not* distinguish between signs of 90 degree phase shifts. However, if phase shift PS is introduced between IF paths, such PD will distinguish between signs of the PD output *voltage* that corresponds to $PS + \Delta\varphi_{IF}$. For instance, if $|PS| = \frac{\pi}{2}$ the PD response takes its maximum positive or negative value when phase difference between its inputs is 0 or 180 degrees.

Therefore, four phase shifters are introduced into the IF paths (Fig. 6) along with two limiting amplifiers which make this part of the circuit less sensitive to the frequency dependencies exhibiting by other components. Having passed through the phase shifters and amplifiers two oscillations are fed into the ports of a simple PD (double balanced mixer ADE-5 by Mini-Circuits). DC blocks prevent operation when $|\Delta f|$ is below 10 MHz.

The net phase shift, theoretically, must lay between 0 and 180 degrees for all possible $|\Delta f|$ values. Naturally, this range of values is to be reduced in practice since HMC520A MMIC does not provide exact quadrature between LO oscillations of its mixers. This discrepancy has been mentioned earlier as $\Delta\varphi_{ref}$. For HMC520A the maximum value of $|\Delta\varphi_{ref}|$ may

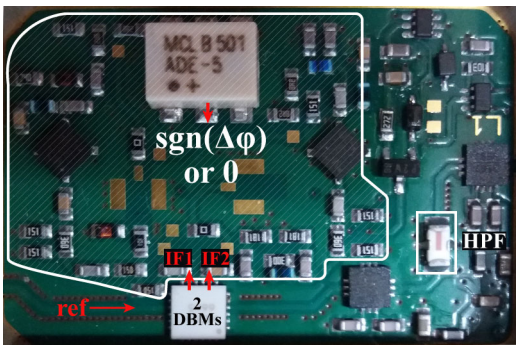

Fig. 5. The photograph of the part of the prototype.

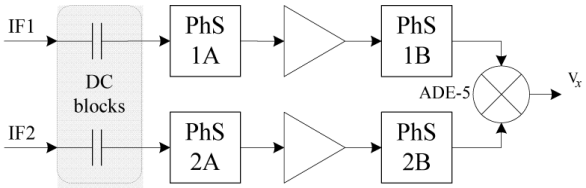

Fig. 6. The phase shift between IF paths (simplified).

be estimated as 20 degrees in the required IF frequency range [4]. Consequently, the net phase shift must lie between 20 and 160 degrees for correct FC operation (Fig. 7).

Now, $sgn\,(\Delta f)$ is in one-to-one correspondence with the sign of the voltage at the ADE-5 IF port V_x. It is then processed in a way to make a response insensitive to $|PS + \Delta\varphi_{IF}|$ variation over frequency. This response exhibits properties of *ternary* logic in controlling current sources connected to the PLL filter (Fig. 8). When $|V_x|$ is large then one of the current sources is turned on, corresponding to the sign of V_x. If $|V_x|$ drops down neither of them is active. Some *delay* is added to the response of this circuit. The need for the delay is explained in the next subsection.

C. Performance

This FC realization showed the pull-in range of 1 GHz with the pull-in time of order of a few microseconds (Fig. 9). However, this performance has been achieved after some adjustment of the delay time (using a simple RC circuit) in the circuitry processing V_x. Without delay periodic switching between pull-up and pull-down states occurred when f_{ref} was switched to 5900 MHz. Also, this effect may be avoided by reducing charge pump currents.

Phase noise of the output oscillation (Fig. 10) was measured with the low noise source (6300 MHz) connected to the reference input. As expected, performance of both oscillations coincide at the offsets well below BW, with noise at other offsets being dominated by the VCO noise.

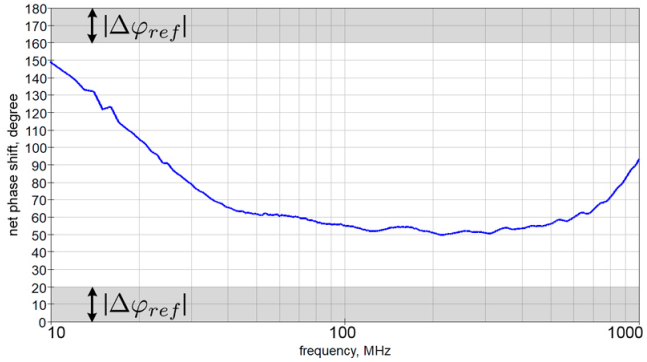

Fig. 7. Net phase shift between IF paths.

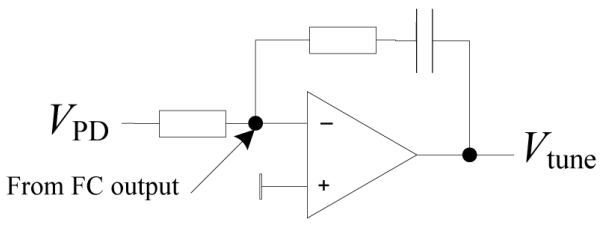

Fig. 8. Connecting current sources to the PLL filter.

Fig. 9. The VCO tuning voltage transient when f_{ref} switched from 5900 MHz to 6900 MHz.

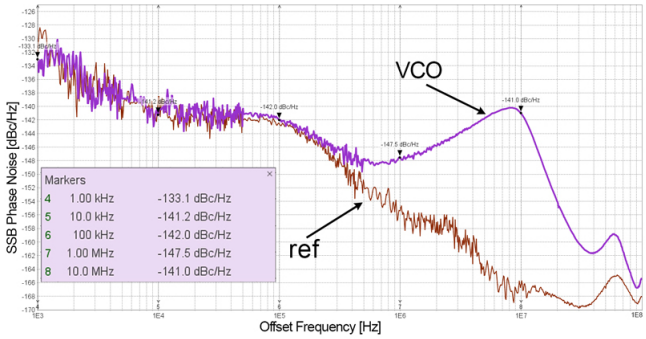

Fig. 10. Phase noise of locked VCO and reference oscillation referred to the output frequency (5600 MHz).

IV. Discussion

A. Survey of pull-in techniques

With the prototype having been measured and, consequently, the approach having been verified, the next step was to appreciate its place among the existing approaches. Therefore, a survey focused on the similar approaches was undertaken. There are only three of them that are relevant.

The approach taken in [1] uses a circuit called quadricorrelator as an AUX. Basically, the quadricorrelator has *linear* response in the vicinity of $|\Delta f| = 0$. This property was originally of importance in *frequency* locked loops. Such property is hardly possible to maintain in the broad range of reference frequencies due to inevitable $\Delta\varphi_{ref}$ deviation from zero. Therefore, this circuit is recommendable only for narrow range tuning applications when careful adjustment of the circuit is possible. Moreover, in [1] and following works the quadricorrelator is always a *distinct* from the PD part of the circuit.

The circuit proposed in [5] may be called a PD and an FC put in digital form. There is evident similarity with the design proposed in this paper. But this circuit is to be realized as an IC consisting of three D-flip-flops which makes a designer *dependable* on IC suppliers. Meanwhile, I/Q mixer MMICs supplied by the market cover the range from roughly 3 GHz up to tens of GHz. Therefore, it may be safely said that the most crucial component for a microwave *analog* FC realization is already generally *available*.

In [6] (pp. 158-161) a circuit called an image rejecting phase detector is proposed to solve a problem commonly arising in a loop with offset. In low noise and low spurious designs

when f_{VCO} is close to the offset frequency, slight change of f_{VCO} may lead to the change of the sign of the VCO detuning, and, consequently, to false responses. Although the detector in [6] distinguishes between positive and negative detuning, it achieves this using a circuit based on a 3PD. So it is inherently *noisy*. An analog FC can deal with the above-mentioned problem and endow a design with its *low* noise performance if up-conversion is substituted for down-conversion.

B. Survey of low noise synthesis techniques

Proliferation of digital PLL ICs made a PLL with the in-loop divider (ILD) a paradigm of frequency synthesis. The division ratio being N, phase noise at the ILD inputs appears multiplied by N^2 at the PLL output. Therefore, any design that *avoids* ILD or, at least, reduces N is claimed to be low noise. Another strategy to reduce pahse noise is to use an *analog* PD which is inherently low noise if compared to a digital PD.

Both ways of phase noise reduction were combined in [7]. There the full 3PD PLL synthesizer is used as an AUX. When the AUX synthesizer is locked, control over the phase is handed to the dividerless PLL with the analog PD. Unfortunately, this approach *lacks* the single 3PD synthesizer *simplicity*, effectively comprising *two* PLLs instead of one.

The other approach with the same downside is given in [8]. The noise produced by the ILD PLL synthesizer is compensated for by means of *another*, but low noise, synthesizer.

C. Conclusion

Among *wideband* PLL synthesizer designs the balance between simplicity and low noise performance has not yet been achieved. Any improvement of the latter is accompanied by inevitable increase in number of spare parts. On the contrary, the PLL design described in this paper is a promising solution to the low noise single PLL synthesis. It is reasonable to envisage that one or two generations of engineers can refine this (yet feeble) design to the degree of perfection characteristic for modern 3PD designs.

Also, it may be helpful for ultra low noise synthesis with frequency offset where the preference to VCOs that are easier to pull in (such as a dielectric resonator oscillator) is given. Usually, both kinds of application mentioned tend to use low f_{ref} which puts stringent requirement on f_{ref} suppression. The proposed technique helps to lessen this requirement providing PLL design with the possibility of choosing higher f_{ref} but without compromising other performance.

ACKNOWLEDGMENT

The author would like to thank his colleagues at Advantex LLC for creating an atmosphere that made this work possible.

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